WHAT IS CLAIMED IS:

1. A device including:

a Network Processor Complex Chip including a plurality of co-processors executing programs that forward frames or hardware assist functions that performs operations like table searches, policing and counting;

a Data Flow Chip operatively coupled to the Network Processor Complex Chip, said Data Flow Chip including at least one port to receive/transmit data and circuit arrangement that sets the at least one port into switch mode and/or line mode; and

a Scheduler Chip operatively coupled to the Data Flow Chip, said Scheduler Chip scheduling frames to meet predetermined Quality of Service commitments.

2. The device of Claim 1 further including a first memory operatively coupled to the Network Processor Complex Chip, a second memory operatively coupled to the Data Flow Chip and a third memory operatively coupled to the Scheduler Chip.

3. A device including:

an ingress section and an egress section symmetrically arranged, said ingress section and said egress section each including

Network Processor Complex Chip having a plurality of co-processors programmed to execute code that forwards network traffic;

a Data Flow Chip operatively coupled to the Network Processor Complex Chip;

said Data Flow Chip having at least one port and circuitry to configure said port into a switch mode or a line mode; and

a Scheduler Chip operatively coupled to said Data Flow Chip, said Scheduler Chip including circuits that schedule frames to meet predetermined Quality of Service commitments.

4. A device including:

an ingress section;

an egress section symmetrically arranged to said ingress section wherein said ingress section includes a First Data Flow Chip having at least a first input port and a first output port;

a First Network Processor Complex Chip operatively coupled to said Data Flow Chip;

a First Scheduler Chip operatively coupled to said Data Flow Chip; and

said egress section including a second Data Flow Chip having at least a second output and a second input;

a second Network Processor Chip operatively coupled to said Second Data Flow Chip;

a second Scheduler Chip operatively coupled to the Second Data Flow Chip; and

communication media that wraps the Second Data Flow Chip to the First Data Flow Chip.

5. The device of Claim 4 further including a Switch interface operatively coupled to the first output port and the second input port.

6. The device of Claim 4 further including a line interface operatively coupled to the first input port and the second output port.

7. A device including:

an ingress section; and

an egress section symmetrically arranged to said ingress section wherein said ingress section includes a First Data Flow Chip having at least a first input port and a first output port;

a First Network Processor Chip operatively coupled to said Data Flow Chip;

a First Scheduler Chip operatively coupled to said Data Flow Chip; and

said egress section including a second Data Flow Chip having at least a second output port and a second input port;

a second Network Processor Chip operatively coupled to said Second Data Flow Chip;

a second Scheduler Chip operatively coupled to the Second Data Flow Chip;

communication media that wraps the Second Data Flow Chip to the First Data Flow Chip;

a first interface operatively coupled to the first output port and the second input port; and

a second interface operatively coupling the first input port and the second output port.

8. A network device including:

a switch fabric and

a plurality of Network Processors connected in parallel to said switch fabric wherein each of the Network Processors including

an ingress section;

an egress section symmetrically arranged to said ingress section wherein said ingress section including a First Data Flow Chip having at least a first input port and a first output port;

a First Network Processor Complex Chip operatively coupled to said first Data Flow Chip;

a First Scheduler Chip operatively coupled to said Data Flow Chip; and

said egress section including a second Data Flow Chip having at least a second output port and a second input port;

a second Network Processor Chip operatively coupled to said Second Data Flow Chip;

a second Scheduler Chip operatively coupled to the Second Data Flow Chip;

communication media that wraps the Second Data Flow Chip to the First Data Flow Chip;

a first interface operatively coupled to the first output port and the second input port; and

a second interface operatively coupling the first input port and the second output port.

9. A Network Processor including:

a Network Processor Complex Chip having a plurality of co-processors;

a memory operatively connected to said Network Processor; and

a Data Flow Chip operatively coupled to said Network Processor Chip, said Data Flow Chip including at least an output port, an input port; and

control mechanism that sets at least the input port or the output port into a switch mode or a line mode.